CSC 462/562 Spring 2019
Tentative Schedule

Week	Readings	Topics
1	Introduction 1.1-1.4, 1.8-1.9, 1.11	Introduction, performance metrics, design concepts
2	No class on Monday (MLK Jr Bday) Appendix A	Instruction set principles RISC-V instruction set and architecture
3	Appendix C (C.1 – C.4)	Introduction to pipelining, RISC-V pipeline
4	Appendix C (C.5 – C.6, C.8)	Extending the RISC-V pipeline, MIPS R4000 pipeline
5	Chapter 3.1-3.3	ILP, loop unrolling, branch prediction
6	Chapter 3.4-3.5	Dynamic scheduling
7	Chapter 3.6-3.8	Hardware-based speculation, superscalars
8	Chapter 3.9-3.13	VLIW, TLP, ARM Cortex
Spring Break Week		
9	Appendix H, chapter 4.5	Additional compiler support, loop-level dependencies
10	Chapter 2.1, 2.3, Appendix B.1-B.3	Memory hierarchy, memory performance, cache optimizations
11	Chapter 2.4, 2.6-2.7, Appendix B.4, B.6	Virtual memory, Cortex-A53 and iCore memory hierarchies
12	Supplemental reading	Intel architectures and microcode
13	Chapter 4.1-4.3	DLP and vector architectures (SIMD)
14	Chapter 4.4, chapter 5.1	GPUs, introduction to MIMD architectures
15	Chapter 5.2-5.4	Shared and distributed memory architectures
Finals Week	Final Exam: Wednesday May 8, 12:20 – 2:20 pm NOTE: even though the final is a take-home assignment, we are required to meet at this time	

All readings are from Computer Architecture: A Quantitative Approach by Hennessy and Patterson (5^{th} edition). Appendix H can be downloaded from the authors' website. Additional material will be provided for week 12's supplemental reading.

Note: The above Schedule is tentative and might change during the semester.